AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A processing device comprising:

one or more resources within a node;

a plurality of peripheral bus interfaces operably coupled to the one or more resources and ~~couple able~~ to couple to a peripheral bus fabric to support resource sharing with a plurality of other processing devices when coupled to the peripheral bus fabric;

a node identification (ID) register programmable to have primary routing resources ~~programmable~~ with a plurality of addresses ~~ranges, the processing device operable~~ to determine a primary routing of a peripheral bus ~~transactions~~ transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction and ~~primary routing resources contents~~ a particular type of transaction; and

~~a~~ the node ID register ~~programmable with a plurality of~~ also to have one or more override indications ~~, the processing device operable~~ to determine an alternate override routing of the peripheral bus ~~transactions~~ transaction among the plurality of peripheral bus interfaces based upon ~~a~~ the destination ~~node ID of the peripheral bus transaction and node ID register contents~~ address and when a type of transaction is other than the particular type of transaction noted for the primary routing.

2. (currently amended) The processing device of claim 1 wherein the processing device determines ~~the~~ a node ID of ~~the~~ a destination processing device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

3. (currently amended) The processing device of claim 1 wherein the processing device

~~may~~ is to ignore the alternate override routing based upon programmed contents of the node ID register ~~contents~~.

4. (currently amended) The processing device of claim 1 wherein the alternate override routing applies to cache coherency peripheral bus transactions.

5. (currently amended) The processing device of claim 1 wherein the alternate override routing applies to input/output peripheral bus transactions.

6. (currently amended) The processing device of claim 1 wherein the alternate override routing applies to both cache coherency peripheral bus transactions and to input/output peripheral bus transactions.

7. (currently amended) The processing device of claim 6, wherein the alternate override routing is selectively disabled ~~able~~ with regard to cache coherency peripheral bus transactions and/or to input/output peripheral bus transactions, in which an override disabled transaction is to use the primary routing.

8. (currently amended) The processing device of claim 6 wherein ~~the override routing does not apply to~~ a packet data peripheral bus ~~transactions~~ transaction is designated for primary routing.

9. (currently amended) The processing device of claim 1, wherein:

~~the override routing relates to one of the plurality of peripheral bus interfaces;~~

the override routing indicates to route the peripheral bus transaction to either a primary port of ~~the~~ an override selected peripheral bus interface or to a secondary port of the override selected peripheral bus interface.

10. (currently amended) The processing device of claim 1 wherein the node ID register comprises an entry for each of a plurality of represented processing devices, each entry comprising:

~~a node ID;~~

an override bit corresponding to input/output peripheral bus transactions;

a primary/secondary port indication corresponding to input/output peripheral bus transactions;

an override bit corresponding to cache coherency peripheral bus transactions; and

a primary/secondary port indication corresponding to cache coherency peripheral bus transactions.

11-28. (canceled)

29. (currently amended) A method for operating a processing device having one or more resources and a plurality of peripheral bus interfaces that are operable to couple the one or more resources to one or more other processing devices via a peripheral bus fabric, the method comprising:

receiving a peripheral bus transaction at the processing device;

determining a primary routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction and ~~primary routing resources contents~~ a particular type of transaction programmed in a node identification (ID) register;

determining an alternate override routing of the peripheral bus ~~transactions~~ transaction among the plurality of peripheral bus interfaces based upon ~~a~~ the ~~destination node ID of the peripheral bus transaction and node ID register contents~~ address and when a type of transaction is other than the particular type of transaction noted for the primary routing, the override routing also programmed in the node ID register; and

routing the peripheral bus transaction among the plurality of peripheral bus interfaces using different paths according to ~~one of~~ the primary routing ~~and~~ or the override routing based on the type of transaction noted for the peripheral bus transaction.

30. (currently amended) The processing device of claim 29 further comprising determining ~~the~~ a node ID of ~~the~~ a destination processing device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

31. (currently amended) The method of claim 29 further comprising choosing to route the peripheral bus transaction according to the primary routing based upon programmed contents of the node ID register ~~contents~~.

32. (currently amended) The method of claim 29 further comprising applying the alternate override routing to cache coherency peripheral bus transactions.

33. (currently amended) The method of claim 29 further comprising applying the alternate override routing to input/output peripheral bus transactions.

34. (currently amended) The method of claim 29 further comprising applying the alternate override routing to both cache coherency peripheral bus transactions and to input/output peripheral bus transactions.

35. (currently amended) The method of claim 34, further comprising applying the primary routing to a packet data peripheral bus ~~transactions~~ transaction.